	L #	Hits	Search Text	DBs
1	L1	14876	(instruction prefetch$3 fetch$3) near5 (queue buffer)	USPAT; US-PGPUB
2	L2	2862	1 near20 cache	USPAT; US-PGPUB
3	L3	1601	1 near50 branch	USPAT; US-PGPUB
4	L4	2224	1 near20 (select$3 multiplex$3)	USPAT; US-PGPUB
5	L7	154	3 near99 4	USPAT; US-PGPUB
6	L8	813	1 near20 target	USPAT; US-PGPUB
7	L12	303	3 near99 8 and 2	USPAT; US-PGPUB
8	L13	242	12 not 7	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040030866 A1	☐	Apparatus and method for buffering instructions and late-generated related information using history of previous load/shifts	712/217
2	US 20040015683 A1	☒	Two dimensional branch history table prefetching mechanism	712/240
3	US 20040003298 A1	☒	Icache and general array power reduction method for loops	713/300
4	US 20040003203 A1	☒	Instruction fetch control device and instruction fetch control method	712/205
5	US 20030226003 A1	☒	Information processor having delayed branch function	712/238
6	US 20030225998 A1	☒	Configurable data processor with multi-length instruction set architecture	712/210
7	US 20030140203 A1	☒	Memory record update filtering	711/159
8	US 20030131212 A1	☒	Absolute address bits kept in branch history table	711/203
9	US 20030070062 A1	☒	System and method for reducing computing system latencies associated with branch instructions	712/234
10	US 20030028758 A1	☒	SINGLE ARRAY BANKED BRANCH TARGET BUFFER	712/238
11	US 20020199092 A1	☒	Split history tables for branch prediction	712/240
12	US 20020194461 A1	☒	Speculative branch target address cache	712/238
13	US 20020143799 A1	☒	Memory record update filtering	707/200
14	US 20020108029 A1	☒	Program counter (PC) relative addressing mode with fast displacement	712/234
15	US 20020095566 A1	☒	METHOD FOR PROCESSING BRANCH OPERATIONS	712/239
16	US 20010054140 A1	☒	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
17	US 20010052053 A1	☒	Stream processing unit for a multi-streaming processor	711/138

	Document ID	U	Title	Current OR
18	US 20010051969 A1	☒	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/514
19	US 20010032309 A1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
20	US 20010027515 A1	☒	Apparatus and method of controlling instruction fetch	712/207
21	US 20010023425 A1	☒	Method and apparatus for rounding in a multiplier arithmetic	708/620
22	US 20010010051 A1	☒	Method and apparatus for multi-function arithmetic	708/502
23	US 6697937 B1	☒	Split history tables for branch prediction	712/240
24	US 6678808 B2	☒	Memory record update filtering	711/159
25	US 6662297 B1	☒	Allocation of processor bandwidth by inserting interrupt servicing instructions to intervene main program in instruction queue mechanism	712/245
26	US 6611910 B2	☒	Method for processing branch operations	712/237
27	US 6604191 B1	☒	Method and apparatus for accelerating instruction fetching for a processor	712/207
28	US 6571331 B2	☒	Static branch prediction mechanism for conditional branch instructions	712/239
29	US 6557098 B2	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
30	US 6553469 B2	☒	Memory record update filtering	711/159
31	US 6546481 B1	☒	Split history tables for branch prediction	712/240
32	US 6532521 B1	☒	Mechanism for high performance transfer of speculative request data between levels of cache hierarchy	711/137
33	US 6513109 B1	☒	Method and apparatus for implementing execution predicates in a computer processing system	712/200
34	US 6510494 B1	☒	Time based mechanism for cached speculative data deallocation	711/137
35	US 6499123 B1	☒	Method and apparatus for debugging an integrated circuit	714/724
36	US 6499101 B1	☒	Static branch prediction mechanism for conditional branch instructions	712/239
37	US 6496921 B1	☒	Layered speculative request unit with instruction optimized and storage hierarchy optimized partitions	712/207
38	US 6487637 B1	☒	Method and system for clearing dependent speculations from a request queue	711/133

	Document ID	U	Title	Current OR
39	US 6477639 B1	☒	Branch instruction mechanism for processor	712/237
40	US 6473833 B1	☒	Integrated cache and directory structure for multi-level caches	711/122
41	US 6453412 B1	☒	Method and apparatus for reissuing paired MMX instructions singly during exception handling	712/244
42	US 6446197 B1	☒	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
43	US 6442681 B1	☒	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
44	US 6438656 B1	☒	Method and system for cancelling speculative cache prefetch requests	711/137
45	US 6427204 B1	☒	Method for just in-time delivery of instructions in a data processing system	712/206
46	US 6427192 B1	☒	Method and apparatus for caching victimized branch predictions	711/133
47	US 6425075 B1	☒	Branch prediction device with two levels of branch prediction cache	712/239
48	US 6421763 B1	☒	Method for instruction extensions for a tightly coupled speculative request unit	711/137
49	US 6421762 B1	☒	Cache allocation policy based on speculative request history	711/130
50	US 6421696 B1	☒	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
51	US 6418516 B1	☒	Method and system for managing speculative requests in a multi-level memory hierarchy	711/138
52	US 6412050 B1	☒	Memory record update filtering	711/159
53	US 6401193 B1	☒	Dynamic data prefetching based on program counter and addressing mode	712/207
54	US 6397239 B2	☒	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/505
55	US 6397238 B2	☒	Method and apparatus for rounding in a multiplier	708/497
56	US 6393554 B1	☒	Method and apparatus for performing vector and scalar multiplication and calculating rounded products	712/221
57	US 6392928 B1	☒	Optimized cache allocation algorithm for multiple speculative requests	711/137
58	US 6392923 B1	☒	Mechanism for invalidating instruction cache blocks in a pipeline processor	711/125
59	US 6381625 B2	☒	Method and apparatus for calculating a power of an operand	708/606
60	US 6374350 B1	☒	System and method of maintaining and utilizing multiple return stack buffers	712/239

	Document ID	U	Title	Current OR
61	US 6374348 B1	☒	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
62	US 6360299 B1	☒	Extended cache state with prefetched stream ID information	711/137
63	US 6356997 B1	☒	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
64	US 6351801 B1	☒	Program counter update mechanism	712/205
65	US 6324643 B1	☒	Branch prediction and target instruction control for processor	712/237
66	US 6311261 B1	☒	Apparatus and method for improving superscalar processors	712/23
67	US 6298367 B1	☒	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/524
68	US 6269384 B1	☒	Method and apparatus for rounding and normalizing results within a multiplier	708/497
69	US 6263427 B1	☒	Branch prediction mechanism	712/236
70	US 6256728 B1	☒	Processor configured to selectively cancel instructions from its pipeline responsive to a predicted-taken short forward branch instruction	712/236
71	US 6256653 B1	☒	Multi-function bipartite look-up table	708/290
72	US 6250821 B1	☒	Method and apparatus for processing branch instructions in an instruction buffer	712/238
73	US 6247124 B1	☒	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
74	US 6247120 B1	☒	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
75	US 6237083 B1	☒	Microprocessor including multiple register files mapped to the same logical storage and inhibiting sychronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
76	US 6233676 B1	☒	Apparatus and method for fast forward branch	712/233
77	US 6223198 B1	☒	Method and apparatus for multi-function arithmetic	708/620
78	US 6223192 B1	☒	Bipartite look-up table with output values having minimized absolute error	708/270
79	US 6216219 B1	☒	Microprocessor circuits, systems, and methods implementing a load target buffer with entries relating to prefetch desirability	712/207
80	US 6212629 B1	☒	Method and apparatus for executing string instructions	712/241
81	US 6199152 B1	☒	Translated memory protection apparatus for an advanced microprocessor	711/207
82	US 6195735 B1	☒	Prefetch circuity for prefetching variable size data	711/204

	Document ID	U	Title	Current OR
83	US 6175897 B1	☒	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
84	US 6170054 B1	☒	Method and apparatus for predicting target addresses for return from subroutine instructions utilizing a return address cache	712/242
85	US 6151671 A	☒	System and method of maintaining and utilizing multiple return stack buffers	712/239
86	US 6144980 A	☒	Method and apparatus for performing multiple types of multiplication including signed and unsigned multiplication	708/627
87	US 6134574 A	☒	Method and apparatus for achieving higher frequencies of exactly rounded results	708/551
88	US 6131104 A	☒	Floating point addition pipeline configured to perform floating point-to-integer and integer-to-floating point conversion operations	708/204
89	US 6115733 A	☒	Method and apparatus for calculating reciprocals and reciprocal square roots	708/654
90	US 6115732 A	☒	Method and apparatus for compressing intermediate products	708/625
91	US 6112019 A	☒	Distributed instruction queue	712/214
92	US 6094668 A	☒	Floating point arithmetic unit including an efficient close data path	708/505
93	US 6088793 A	☒	Method and apparatus for branch execution on a multiple-instruction-set-architecture microprocessor	712/239
94	US 6088715 A	☒	Close path selection unit for performing effective subtraction within a floating point arithmetic unit	708/505
95	US 6085213 A	☒	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and summing the products	708/603
96	US 6085212 A	☒	Efficient method for performing close path subtraction in a floating point arithmetic unit	708/505
97	US 6085208 A	☒	Leading one prediction unit for normalizing close path subtraction results within a floating point arithmetic unit	708/205
98	US 6067616 A	☒	Branch prediction device with two levels of branch prediction cache	712/239
99	US 6065110 A	☒	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
100	US 6058465 A	☒	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
101	US 6052708 A	☒	Performance monitoring of thread switch events in a multithreaded processor	718/108
102	US 6044459 A	☒	Branch prediction apparatus having branch target buffer for effectively processing branch instruction	712/237
103	US 6038583 A	☒	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and calculating a rounded products	708/628
104	US 6035386 A	☒	Program counter update mechanism	712/205
105	US 6031992 A	☒	Combining hardware and software to provide an improved microprocessor	717/138

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106	US 6029244 A	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
107	US 6029228 A	☒	Data prefetching of a load target buffer for post-branch instructions based on past prediction accuracy's of branch predictions	711/137
108	US 6026483 A	☒	Method and apparatus for simultaneously performing arithmetic on two or more pairs of operands	712/221
109	US 6012125 A	☒	Superscalar microprocessor including a decoded instruction cache configured to receive partially decoded instructions	711/125
110	US 6011908 A	☒	Gated store buffer for an advanced microprocessor	714/19
111	US 5996071 A	☒	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
112	US 5978896 A	☒	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23
113	US 5974260 A	☒	Data processor to control a sequence of instructions to be executed by rearranging the instruction blocks	712/32
114	US 5964868 A	☒	Method and apparatus for implementing a speculative return stack buffer	712/234
115	US 5958061 A	☒	Host microprocessor with apparatus for temporarily holding target processor state	714/1
116	US 5954815 A	☒	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
117	US 5953512 A	☒	Microprocessor circuits, systems, and methods implementing a loop and/or stride predicting load target buffer	712/205
118	US 5951679 A	☒	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
119	US 5946705 A	☒	Avoidance of cache synonyms	711/108
120	US 5944818 A	☒	Method and apparatus for accelerated instruction restart in a microprocessor	712/244
121	US 5941983 A	☒	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issurance of instructions from the queues	712/214
122	US 5941980 A	☒	Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system	712/204
123	US 5931944 A	☒	Branch instruction handling in a self-timed marking system	712/239
124	US 5926832 A	☒	Method and apparatus for aliasing memory data in an advanced microprocessor	711/141
125	US 5926053 A	☒	Selectable clock generation mode	327/298
126	US 5918062 A	☒	Microprocessor including an efficient implemention of an accumulate instruction	712/7
127	US 5918046 A	☒	Method and apparatus for a branch instruction pointer table	712/239

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128	US 5909566 A	☒	Microprocessor circuits, systems, and methods for speculatively executing an instruction using its most recently used data while concurrently prefetching data for the instruction	712/207
129	US 5898866 A	☒	Method and apparatus for counting remaining loop instructions and pipelining the next instruction	712/241
130	US 5896493 A	☒	Raid algorithm using a multimedia functional unit	714/6
131	US 5892249 A	☒	Integrated circuit having reprogramming cell	257/209
132	US 5870612 A	☒	Method and apparatus for condensed history buffer	710/260
133	US 5867683 A	☒	Method of operating a high performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
134	US 5867682 A	☒	High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations	712/210
135	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
136	US 5860096 A	☒	Multi-level instruction cache for a computer	711/122
137	US 5860014 A	☒	Method and apparatus for improved recovery of processor state using history buffer	710/260
138	US 5857089 A	☒	Floating point stack and exchange instruction	712/222
139	US 5850543 A	☒	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
140	US 5848268 A	☒	Data processor with branch target address generating unit	712/233
141	US 5842008 A	☒	Method and apparatus for implementing a branch target buffer cache with multiple BTB banks	712/240
142	US 5838984 A	☒	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
143	US 5838944 A	☒	System for storing processor register data after a mispredicted branch	712/218
144	US 5835967 A	☒	Adjusting prefetch size based on source of prefetch address	711/213
145	US 5835951 A	☒	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
146	US 5832259 A	☒	Apparatus for superscalar instruction pre-decoding using cached instruction lengths	712/238
147	US 5832205 A	☒	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed	714/53
148	US 5822576 A	☒	Branch history table with branch pattern field	712/239
149	US 5819056 A	☒	Instruction buffer organization method and system	712/204

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150	US 5815693 A	☒	Processor having a frequency modulated core clock based on the criticality of program activity	713/501
151	US 5815692 A	☒	Distributed clock generator	713/501
152	US 5812839 A	☒	Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit	712/239
153	US 5805878 A	☒	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
154	US 5805853 A	☒	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
155	US 5799162 A	☒	Program counter update mechanism	712/205
156	US 5781783 A	☒	Method and apparatus for dynamically adjusting the power consumption of a circuit block within an integrated circuit	713/320
157	US 5781753 A	☒	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
158	US 5778435 A	☒	History-based prefetch cache including a time queue	711/137
159	US 5778246 A	☒	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
160	US 5774710 A	☒	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
161	US 5768576 A	☒	Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor	712/238
162	US 5768575 A	☒	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
163	US 5765220 A	☒	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
164	US 5764970 A	☒	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
165	US 5764938 A	☒	Resynchronization of a superscalar processor	712/200
166	US 5761490 A	☒	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
167	US 5758120 A	☒	Method and system for increased system memory concurrency in a multi-processor computer system utilizing concurrent access of reference and change bits	711/150
168	US 5751981 A	☒	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
169	US 5748932 A	☒	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
170	US 5740419 A	☒	Processor and method for speculatively executing an instruction loop	712/241

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171	US 5740417 A	☒	Pipelined processor operating in different power mode based on branch prediction state of branch history bit encoded as taken weakly not taken and strongly not taken states	712/239
172	US 5740416 A	☒	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
173	US 5740415 A	☒	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
174	US 5740410 A	☒	Static clock generator	713/501
175	US 5740392 A	☒	Method and apparatus for fast decoding of 00H and OFH mapped instructions	712/210
176	US 5740391 A	☒	Preventing premature early exception signaling with special instruction encoding	712/200
177	US 5737750 A	☒	Partitioned single array cache memory having first and second storage regions for storing non-branch and branch instructions	711/129
178	US 5737590 A	☒	Branch prediction system using limited branch target buffer updates	712/238
179	US 5734881 A	☒	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
180	US 5732253 A	☒	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
181	US 5732243 A	☒	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
182	US 5727177 A	☒	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
183	US 5721855 A	☒	Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer	712/218
184	US 5721854 A	☒	Method and apparatus for dynamic conversion of computer instructions	712/203
185	US 5717892 A	☒	Selectively operable cache memory	711/128
186	US 5706491 A	☒	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
187	US 5701448 A	☒	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
188	US 5696955 A	☒	Floating point stack and exchange instruction	712/222
189	US 5692168 A	☒	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
190	US 5692167 A	☒	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
191	US 5687349 A	☒	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
192	US 5664136 A	☒	High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations	712/208
193	US 5655098 A	☒	High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format	712/210

	Document ID	U	Title	Current OR
194	US 5655097 A	☒	High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format	712/204
195	US 5651125 A	☒	High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
196	US 5649225 A	☒	Resynchronization of a superscalar processor	712/23
197	US 5649145 A	☒	Data processor processing a jump instruction	711/213
198	US 5649137 A	☒	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
199	US 5634103 A	☒	Method and system for minimizing branch misprediction penalties within a processor	712/235
200	US 5632023 A	☐	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218

	Document ID	U	Title	Current OR
1	US 20040 00321 6 A1	☐	Branch prediction apparatus and method	712/237
2	US 20040 00320 2 A1	☒	Instruction fetch control apparatus	712/205
3	US 20030 20470 5 A1	☒	Prediction of branch instructions in a data processing apparatus	712/207
4	US 20030 09754 9 A1	☒	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/240
5	US 20030 00526 2 A1	☒	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
6	US 20030 00468 3 A1	☒	Instruction pre-fetching mechanism for a multithreaded program execution	702/186
7	US 20020 19909 1 A1	☒	Apparatus for branch prediction based on history table	712/240
8	US 20020 18880 8 A1	☒	Random generator	711/133
9	US 20020 14408 7 A1	☒	Architecture of method for fetching microprocessor's instructions	712/207
10	US 20020 12082 9 A1	☒	Data processer and data processing system	712/207
11	US 20020 09991 0 A1	☒	High speed low power cacheless computer system	711/117
12	US 20020 09191 6 A1	☒	Embedded-DRAM-DSP architecture	712/228
13	US 20020 08784 5 A1	☒	Embedded-DRAM-DSP architecture	712/228
14	US 20020 04042 9 A1	☒	Embedded-DRAM-DSP architecture	712/228
15	US 20020 01389 4 A1	☒	Data processor with branch target buffer	712/238
16	US 20010 05413 7 A1	☒	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11
17	US 20010 04746 7 A1	☒	METHOD AND APPARATUS FOR BRANCH PREDICTION USING FIRST AND SECOND LEVEL BRANCH PREDICTION TABLES	712/228

	Document ID	U	Title	Current OR
18	US 20010037444 A1	☒	INSTRUCTION BUFFERING MECHANISM	712/207
19	US 20010018735 A1	☒	Data processor and data processing system	712/207
20	US 6701426 B1	☒	Switching between a plurality of branch prediction processes based on which instruction set is operational wherein branch history data structures are the same for the plurality of instruction sets	712/239
21	US 6687857 B1	☒	Microcomputer which can execute a monitor program supplied from a debugging tool	714/38
22	US 6511 62 B1	☒	Recursively accessing a branch target address cache using a target address previously accessed from the branch target address cache	712/238
23	US 6647467 B1	☒	Method and apparatus for high performance branching in pipelined microsystems	711/140
24	US 6631464 B1	☒	Instruction pipeline with a branch prefetch when the branch is certain	712/234
25	US 6622236 B1	☒	Microprocessor instruction fetch unit for processing instruction groups having multiple branch instructions	712/206
26	US 6609194 B1	☒	Apparatus for performing branch target address calculation based on branch type	712/238
27	US 6598154 B1	☒	Precoding branch instructions to reduce branch-penalty in pipelined processors	712/237
28	US 6598153 B1	☒	Processor and method that accelerate evaluation of pairs of condition-setting and branch instructions	712/234
29	US 6598152 B1	☒	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
30	US 6581120 B1	☒	Interrupt controller	710/262
31	US 6553488 B2	☒	Method and apparatus for branch prediction using first and second level branch prediction tables	712/239
32	US 6553480 B1	☒	System and method for managing the execution of instruction groups having multiple executable instructions	712/23
33	US 6542982 B2	☒	Data processer and data processing system	712/207
34	US 6530016 B1	☒	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/237
35	US 6523110 B1	☒	Decoupled fetch-execute engine with static branch prediction support	712/239
36	US 6505292 B1	☒	Processor including efficient fetch mechanism for L0 and L1 caches	712/207
37	US 6502188 B1	☒	Dynamic classification of conditional branches in global history branch prediction	712/234
38	US 6477640 B1	☒	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
39	US 6470443 B1	☒	Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information	712/205

	Document ID	U	Title	Current OR
40	US 6457117 B1	☒	Processor configured to predecode relative control transfer instructions and replace displacements therein with a target address	712/213
41	US 6434691 B1	☒	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
42	US 6418525 B1	☒	Method and apparatus for reducing latency in set-associative caches using set prediction	711/213
43	US 6389531 B1	☒	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
44	US 6367006 B1	☒	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
45	US 6367001 B1	☒	Processor including efficient fetch mechanism for L0 and L1 caches	712/205
46	US 6292884 B1	☒	Reorder buffer employing last in line indication	712/216
47	US 6253316 B1	☒	Three state branch history using one bit in a branch prediction mechanism	712/239
48	US 6216206 B1	☒	Trace victim cache	711/133
49	US 6199154 B1	☒	Selecting cache to fetch in multi-level cache system based on fetch address source and pre-fetching additional data to the cache for future access	712/205
50	US 6170038 B1	☒	Trace based instruction caching	711/125
51	US 6167506 A	☒	Replacing displacement in control transfer instruction with encoding indicative of target address, including offset and target cache line location	712/213
52	US 6157998 A	☒	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
53	US 6157988 A	☒	Method and apparatus for high performance branching in pipelined microsystems	711/140
54	US 6134649 A	☒	Control transfer indication in predecode which identifies control transfer instruction and an alternate feature of an instruction	712/204
55	US 6122729 A	☒	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
56	US 6119222 A	☒	Combined branch prediction and cache prefetch in a microprocessor	712/238
57	US 6119205 A	☒	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
58	US 6108775 A	☒	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
59	US 6098167 A	☒	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
60	US 6076144 A	☒	Method and apparatus for identifying potential entry points into trace segments	711/125
61	US 6073213 A	☒	Method and apparatus for caching trace segments with multiple entry points	711/125
62	US 6073159 A	☒	Thread properties attribute vector based thread selection in multithreading processor	718/103

	Document ID	U	Title	Current OR
63	US 6061786 A	☒	Processor configured to select a next fetch address by partially decoding a byte of a control transfer instruction	712/237
64	US 6038659 A	☒	Method for using read-only memory to generate controls for microprocessor	712/226
65	US 6035387 A	☒	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
66	US 6032251 A	☒	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
67	US 6021489 A	☒	Apparatus and method for sharing a branch prediction unit in a microprocessor implementing a two instruction set architecture	712/239
68	US 6018786 A	☒	Trace based instruction caching	711/4
69	US 6003142 A	☒	Test facilitating circuit of microprocessor	714/30
70	US 5948100 A	☒	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
71	US 5944817 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/240
72	US 5935241 A	☒	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
73	US 5922068 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215
74	US 5918045 A	☒	Data processor and data processing system	712/237
75	US 5918044 A	☒	Apparatus and method for instruction fetching using a multi-port instruction cache directory	712/235
76	US 5913049 A	☒	Multi-stream complex instruction set microprocessor	712/215
77	US 5913048 A	☒	Dispatching instructions in a processor supporting out-of-order execution	712/215
78	US 5903751 A	☒	Method and apparatus for implementing a branch target buffer in CISC processor	712/238
79	US 5899986 A	☒	Instruction fetch unit including instruction buffer and secondary or branch target buffer that transfers prefetched instructions to the instruction buffer	712/237
80	US 5887161 A	☒	Issuing instructions in a processor supporting out-of-order execution	712/244
81	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
82	US 5881260 A	☒	Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction	712/210
83	US 5867698 A	☒	Apparatus and method for accessing a branch target buffer	712/238
84	US 5864697 A	☒	Microprocessor using combined actual and speculative branch history prediction	712/240
85	US 5848269 A	☒	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239

	Document ID	U	Title	Current OR
86	US 5845099 A	☒	Length detecting unit for parallel processing of variable sequential instructions	712/204
87	US 5835705 A	☒	Method and system for performance per-thread monitoring in a multithreaded processor	714/47
88	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
89	US 5809320 A	☒	High-performance multi-processor having floating point unit	712/34
90	US 5809294 A	☒	Parallel processing unit which processes branch instructions without decreased performance when a branch is taken	712/233
91	US 5805475 A	☒	Load-store unit and method of loading and storing single-precision floating-point registers in a double-precision architecture	708/204
92	US 5796998 A	☒	Apparatus and method for performing branch target address calculation and branch prediciton in parallel in an information handling system	712/239
93	US 5794027 A	☒	Method and apparatus for managing the execution of instructons with proximate successive branches in a cache-based data processing system	712/238
94	US 5784604 A	☒	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
95	US 5768555 A	☒	Reorder buffer employing last in buffer and last in line bits	712/216
96	US 5764940 A	☒	Processor and method for executing a branch instruction and an associated target instruction utilizing a single instruction fetch	712/206
97	US 5752014 A	☒	Automatic selection of branch prediction methodology for subsequent branch instruction based on outcome of previous branch prediction	712/240
98	US 5748976 A	☒	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
99	US 5732005 A	☒	Single-precision, floating-point register array for floating-point units performing double-precision operations by emulation	708/495
100	US 5715440 A	☒	Branch instruction executing device for tracing branch instruments based on instruction type	712/233
101	US 5715420 A	☒	Method and system for efficient memory management in a data processing system utilizing a dual mode translation lookaside buffer	711/206
102	US 5706492 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/238
103	US 5699538 A	☒	Efficient firm consistency support mechanisms in an out-of-order execution superscaler multiprocessor	712/23
104	US 5671382 A	☒	Information processing system and information processing method for executing instructions in parallel	712/215
105	US 5668985 A	☒	Decoder having a split queue system for processing intstructions in a first queue separate from their associated data processed in a second queue	712/245
106	US 5644744 A	☒	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
107	US 5642500 A	☒	Method and apparatus for controlling instruction in pipeline processor	712/233
108	US 5640526 A	☒	Superscaler instruction pipeline having boundary indentification logic for variable length instructions	712/207

	Document ID	U	Title	Current OR
109	US 5634136 A	☒	Data processor and method of controlling the same	712/237
110	US 5634047 A	☒	Method for executing branch instructions by processing loop end conditions in a second processor	712/241
111	US 5625787 A	☒	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
112	US 5625785 A	☒	Information processing apparatus having dual buffers for transmitting debug data to an external debug unit	712/227
113	US 5623615 A	☒	Circuit and method for reducing prefetch cycles on microprocessors	712/238
114	US 5574871 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/200
115	US 5511172 A	☒	Speculative execution processor	712/235
116	US 5509130 A	☒	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
117	US 5488730 A	☒	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
118	US 5481689 A	☒	Conversion of internal processor register commands to I/O space addresses	711/202
119	US 5471591 A	☒	Combined write-operand queue and read-after-write dependency scoreboard	712/217
120	US 5454087 A	☒	Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT	712/240
121	US 5450555 A	☒	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
122	US 5442756 A	☒	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
123	US 5418917 A	☒	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
124	US 5414822 A	☒	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
125	US 5394529 A	☒	Branch prediction unit for high-performance processor	712/240
126	US 5386519 A	☒	Information processing apparatus incorporating buffer storing a plurality of branch target instructions for branch instructions and interrupt requests	712/238
127	US 5381532 A	☒	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
128	US 5367703 A	☒	Method and system for enhanced branch history prediction accuracy in a superscalar processor system	712/23
129	US 5333296 A	☒	Combined queue for invalidates and return data in multiprocessor system	711/171
130	US 5317720 A	☒	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143

	Document ID	U	Title	Current OR
131	US 52874 67 A	☒	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
132	US 52838 73 A	☒	Next line prediction apparatus for a pipelined computed system	712/207
133	US 52652 13 A	☒	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
134	US 51971 36 A	☒	Processing system for branch instruction	712/238
135	US 51558 43 A	☒	Error transition mode for multi-processor system	714/5
136	US 51519 80 A	☒	Buffer control circuit for data processor	712/237
137	US 51270 91 A	☒	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
138	US 50994 19 A	☒	Pipeline microcomputer having branch instruction detector and bus controller for producing and carrying branch destination address prior to instruction execution	712/233
139	US 50500 76 A	☒	Prefetching queue control system	712/219
140	US 49929 32 A	☒	Data processing device with data buffer control	712/237
141	US 49910 80 A	☒	Pipeline processing apparatus for executing instructions in three streams, including branch stream pre-execution processor for pre-executing conditional branch instructions	712/206
142	US 49531 21 A	☒	Circuitry for and method of controlling an instruction buffer in a data-processing system	712/241
143	US 49439 08 A	☒	Multiple branch analyzer for prefetching cache lines	712/240
144	US 49425 25 A	☒	Data processor for concurrent executing of instructions by plural execution units	712/217
145	US 48274 02 A	☒	Branch advanced control apparatus for advanced control of a branch instruction in a data processing system	712/234
146	US 47424 51 A	☒	Instruction prefetch system for conditional branch instruction for central processor unit	712/235
147	US 47259 47 A	☒	Data processor with a branch target instruction storage	712/238
148	US 46791 41 A	☒	Pageable branch history table	712/240
149	US 46046 91 A	☒	Data processing system having branch instruction prefetching performance	712/207
150	US 43375 10 A	☒	Read control system for a control storage device	712/211
151	US 42009 27 A	☒	Multi-instruction stream branch processing mechanism	712/235
152	US 40015 68 A	☒	Monetary receipt and payment managing apparatus	705/43
153	US 37711 38 A	☒	APPARATUS AND METHOD FOR SERIALIZING INSTRUCTIONS FROM TWO INDEPENDENT INSTRUCTION STREAMS	712/205

	Document ID	U	Title	Current OR
154	US 3614747 A	☐	INSTRUCTION BUFFER SYSTEM	711/125

	L #	Hits	Search Text	DBs
1	L1	14876	(instruction prefetch$3 fetch$3) near5 (queue buffer)	USPAT; US-PGPUB
2	L2	2862	1 near20 cache	USPAT; US-PGPUB
3	L3	1601	1 near50 branch	USPAT; US-PGPUB
4	L4	2224	1 near20 (select$3 multiplex$3)	USPAT; US-PGPUB
5	L8	813	1 near20 target	USPAT; US-PGPUB
6	L12	303	3 near99 8 and 2	USPAT; US-PGPUB
7	L13	242	12 not 7	USPAT; US-PGPUB
8	L7	154	3 near99 4	USPAT; US-PGPUB
9	L14	5468	(instruction prefetch$3 fetch$3) near5 (queue buffer)	EPO; JPO; DERWENT; IBM_TDB
10	L15	362	14 near20 cache	EPO; JPO; DERWENT; IBM_TDB
11	L16	377	14 near20 branch	EPO; JPO; DERWENT; IBM_TDB
12	L17	163	14 near20 target	EPO; JPO; DERWENT; IBM_TDB
13	L18	474	14 near20 (select$3 multiplex$3)	EPO; JPO; DERWENT; IBM_TDB
14	L22	88	15 and (16 17 18)	EPO; JPO; DERWENT; IBM_TDB
15	L23	67	15 near20 (line block)	EPO; JPO; DERWENT; IBM_TDB
16	L24	11	23 and branch	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 2002229778 A	☐	PC RELATIVE BRANCHING METHOD WITH HIGH-SPEED DISPLACEMENT	
2	JP 2002108703 A	☒	CACHE CONTROLLER AND PROCESSOR	
3	JP 2000357090 A	☒	MICROCOMPUTER AND CACHE CONTROL METHOD	
4	JP 2000215053 A	☒	CONVERTING METHOD FOR INSTRUCTION STREAM	
5	JP 2000215048 A	☒	CONVERTING METHOD FOR INSTRUCTION STREAM	
6	JP 2000132391 A	☒	BRANCH PREDICTION MECHANISM	
7	JP 11316681 A	☒	LOADING METHOD TO INSTRUCTION BUFFER AND DEVICE AND PROCESSOR THEREFOR	
8	JP 11272467 A	☒	METHOD FOR OPERATING SUPERSCALAR PROCESSOR AND CIRCUIT DEVICE	
9	JP 11073402 A	☒	BUS BRIDGE CIRCUIT	
10	JP 10214188 A	☒	METHOD FOR SUPPLYING INSTRUCTION OF PROCESSOR, AND DEVICE THEREFOR	
11	JP 09091136 A	☒	SIGNAL PROCESSOR	
12	JP 09034786 A	☒	INSTRUCTION SUPPLYING DEVICE	
13	JP 08190482 A	☒	METHOD AND DEVICE FOR SCANNING INSTRUCTION QUEUE	
14	JP 08077000 A	☒	CIRCUIT AND METHOD TO REDUCE POWER CONSUMPTION OF SUPER SCALAR PROCESSOR	
15	JP 08069411 A	☒	SEMICONDUCTOR DEVICE	
16	JP 08044563 A	☒	MICROPROCESSOR	
17	JP 08016468 A	☒	DATA PREFETCH CONTROL CIRCUIT	
18	JP 08006853 A	☒	STORAGE CONTROL METHOD	
19	JP 07210383 A	☒	MECHANISM AND METHOD FOR PREDICTING BRANCHING INSTRUCTION	
20	JP 07182163 A	☒	SUPER-SCALAR INSTRUCTION DECODING/ISSUING DEVICE	
21	JP 07105002 A	☒	COMPUTER SYSTEM	

	Document ID	U	Title	Current OR
22	JP 07073 104 A	☒	SYSTEM AND METHOD FOR MANAGING EXECUTION OF INSTRUCTION INCLUDING PROXIMATED BRANCHING INSTRUCTION	
23	JP 06110 683 A	☒	METHOD AND DEVICE FOR EXTENDED BRANCH TARGET OF MICROPROCESSOR	
24	JP 05158 689 A	☒	BRANCHING PREDICTION DEVICE	
25	JP 04227 542 A	☒	INFORMATION PROCESSOR	
26	JP 04188 245 A	☒	CACHE MEMORY CONTROLLER	
27	JP 04148 428 A	☒	MICRO PROCESSOR INTEGRATED CIRCUIT	
28	JP 02239 330 A	☒	INFORMATION PROCESSOR	
29	JP 01088 844 A	☒	DATA PROCESSOR	
30	JP 63163 532 A	☒	MICROPROCESSOR	
31	JP 59079 482 A	☒	CACHE MEMORY CONTROL SYSTEM	
32	EP 69765 0 A2	☒	Apparatus and method for instruction queue scanning	
33	EP 64908 6 A1	☒	Microprocessor with speculative execution.	
34	WO 93173 84 A1	☒	CPU HAVING PIPELINED INSTRUCTION UNIT AND EFFECTIVE ADDRESS CALCULATION UNIT WITH RETAINED VIRTUAL ADDRESS CAPABILITY	
35	EP 52218 6 A1	☒	Demultiplexer.	
36	EP 47759 8 A2	☒	Instruction unit for a processor featuring 'n' processing elements.	
37	EP 47143 4 A2	☒	Methods and apparatus for controlling a multi-segment cache memory.	
38	EP 47073 6 A1	☒	Cache memory system.	
39	EP 45740 3 A2	☒	Multilevel instruction cache, method for using said cache, method for compiling instructions for said cache and micro computer system using such a cache.	
40	EP 27118 7 A2	☒	Split instruction and operand cache management.	
41	US 66474 67 B	☒	Branch caching and pipeline controlling method for very long instruction word digital signal processor, involves caching contents of variable number of immediately following prefetch buffers	
42	TW 53837 4 A	☒	Instruction cache device and method using instruction read buffer - for increasing probability of instruction hit to efficiently access the instruction word in cache instruction word memory	
43	US 66041 91 B	☒	Instruction fetching system for microprocessor, fetches instruction from sum-addressed instruction cache to provide both target and inline paths	

	Document ID	U	Title	Current OR
44	US 20030 10594 6 A	☒	Microprocessor selects one copy of broadcast state based on identifier set in microinstruction by microcode sequencer, to process microinstruction	
45	US 65534 83 B	☒	Register allocation unit for processing system, has controller to generate hit signal when new input value matches value stored in value cache	
46	WO 20027 7822 A	☒	Monitoring run time execution of software code by inserting routine into buffer with data or cache disabling instruction	
47	US 64271 89 B	☒	Multi-level cache structure for computer processor, issues predetermined number of entries from data or instruction queues in consecutive clock cycles	
48	US 63670 06 B	☒	Multiprocessor for computer system, selects next prefetch buffer in response to buffer pointer in previous predecoded buffer	
49	JP 20011 66989 A	☒	Memory system for computer, performs prefetch of address data relating to prefetch start position of target data, from main memory and stores it in prefetch buffer	
50	US 62232 58 B	☒	Processor for computer system, has detector circuit to recognize cacheable and non-cacheable instruction based on which bus request is output for allocating buffers	
51	US 62090 58 B	☒	Data transfer between data disk and cache buffer in cache memory system, involves delaying reading process until pre-fetch data area rotates under transducer, if landing position is outside the data segment	
52	US 61856 69 B	☒	Hardware embedded run-time optimizer, using Instruction Pointer to Trace Memory (IP-to-TM) cache to map branch targets to optimize traces and determines match by parallel examination of cache and Instruction Translation Lookup Buffer (ITLB)	
53	US 61758 97 B	☒	Data processing system for pipelined computer central processor, sends instruction to pipeline from instruction buffer, if buffer target address matches with transfer instruction target address	
54	JP 20003 57090 A	☒	Microcomputer has built-in branch estimation mechanism to reduce access time when cache mistake occurs and precoder to judge branch instruction to be executed	
55	US 61548 33 A	☒	Branch target buffer hardware conflict handling method in electronic system, involves invalidating instruction pointer associated with branch target buffer cache read that is suppressed due to write allocation	
56	US 60731 59 A	☒	Multithreading processor selects attributes of threads by locating instruction in proximity with head of instruction queue	
57	US 60121 34 A	☒	Instruction prefetching apparatus between caches of high speed processor	
58	CN 12260 24 A	☒	Instruction buffer loading method for superscalar processor, involves assigning fetch address to specific slot of instruction buffer, in which first instruction from cache is stored	
59	EP 93653 9 A	☒	Process of fetching commands for programmed controlled unit, microprocessor, micro-controller - selectively branches to specific locations in instruction queue when writing instruction data to queue and/or reading instruction data from queue	
60	US 58420 08 A	☒	Branch target buffer circuit for microprocessor - has branch prediction circuit that indexes all ordered branch target buffer banks of buffer cache, using instruction pointer	
61	US 58227 90 A	☒	Voting data prefetch system - includes voter coupled to prefetch buffer and selects prefetch address from one of two prefetch predictors based on prediction efficacies, to retrieve data from buffer	

	Document ID	U	Title	Current OR
62	US 5802594 A	☒	Instruction translation look-aside buffer for cache of microprocessor - precharges each of hit line during first phase of clock cycle and matches and selects physical address in second phase of cycle	
63	US 5796998 A	☒	Instructions fetching apparatus for information handling system - has branch address calculator to which branch queue is coupled for receiving target addresses and addresses of set of fetched instructions	
64	JP 10198561 A	☒	Microprocessor using multi-level memory system - has load target buffer containing second entries, which include value which makes second corresponding data fetch instructions correspond to second entry, prevented from producing pre-fetch demand	
65	US 5754811 A	☒	Instruction dispatch queue - includes circular dispatch queue with dispatch sequence logic coupled to bottom of dispatch queue pointer for controlling multiplexers so queue outputs instruction from queue to execution unit	
66	US 5734881 A	☒	Short Change-Of-Flow detection scheme processor for detecting COF instruction and target instruction are in pre-fetch buffer - has Branch Target Cache which outputs target data in accessed COF entry to pre-fetch unit, and pre-fetch unit which suppresses issue of corresp pre-fetch address if pre-fetch buffer field is valid	
67	EP 927394 B	☒	Branch prediction for a microprocessor instruction cache - has a branch target buffer which shares locations among sets of an instruction cache to store branch information for multiple branch instructions, when a cache line of a set stores more than one branch instruction	
68	JP 09146835 A	☒	Data processing system is microprocessor - includes control circuit connected to filter circuit, which controls fetch and prefetch state of buffer circuit from first and second cache memory selectively	
69	JP 09091136 A	☒	Signal processing appts for command loop processing - has buffer which is used to store and output instruction to be executed in command loop till end of loop when command cache takes over	
70	JP 08320788 A	☒	Pipeline processor for microcomputers - incorporates branch point buffer to monitor and fetch the branched address instruction from cache memory	
71	JP 08286914 A	☒	Memory control device for information processing appts - has control unit which determines address of pre memory block which performs next fetch, based on output of decoding unit	
72	US 5553254 A	☒	First-in-first-out queue for managing instruction sequence execution - has fields provided in queue element structure for referencing correct instruction cache line but also for specifying cache line sub-sequences and location of branch instructions	
73	EP 718758 A	☒	Cache control unit - includes boundary identification logic to determine nature of byte and anticipation buffer loaded with sequentially anticipated prefetched instructions	
74	JP 08077000 A	☒	Computer memory system super scalar microprocessor - has pre-prohibition circuit that controls execution circuit so that pre-buffer corresp. to pre-prohibition signal from cache command is forbidden	
75	US 5515521 A	☒	Microprocessor access control unit with fetch address queue - has circuit postponing pending fetch requests from CPU to allow high-priority requests with state machine to provide control signal to address selector	
76	GB 2285526 A	☒	Branch instruction prediction mechanism for pipelined microprocessors - addresses information stored by last byte of each branch instruction and sends instruction pointer to branch target buffer circuit when computer fetches block of instructions	
77	US 5335330 A	☒	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
78	US 5499355 A	☒	Fast memory access system - has cache memory containing selected data obtained from main memory and buffer storing data that is prefetched before next read request	

	Document ID	U	Title	Current OR
79	EP 628184 B	☒	Digital data processor instruction pre-fetch unit - has branch history table indicates occurrence of branch instruction having target address that was previously taken	
80	EP 522186 A	☒	Multiplexer for cache memories or instruction buffers - selects several adjacent bits, such as four out of sixteen, bytes, half words or words from one register and places them in same order in second register	
81	US 5168560 A	☒	Microprocessor system with split operand and instructions cache tag stores - has system tag store with different validity bit for same data line	
82	EP 471434 A	☒	Multi segment cache memory controller - has cache memory segmented to operate at selected working segmentation level	
83	US 5230068 A	☒	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	
84	US 4926323 A	☒	Streamlined instruction processor for pipelined data - shares address bus between instruction and data accesses with bus being released before transfer is connected	
85	EP 351955 A	☒	Multiprocessor system with cross-interrogated store-in-cache control - uses fetch buffer selectively coupled between memory and requesting processor	
86	EP 348652 A	☒	Checkpoint retry system for processors with cache - has cache pages saved in store buffers following checkpoint	
87	US 4847753 A	☒	Pipelined processing instructions computer - compares predicted target address in cache with real target upon branch instruction execution	
88	AU 8779840 A	☐	Data transfer management system for multiple CPU architecture - implements split instruction and operand cache line-pair state control when program instructions and data are mixed in application program	

	Document ID	U	Title	Current OR
1	JP 2000132391 A	☐	BRANCH PREDICTION MECHANISM	
2	JP 63163532 A	☒	MICROPROCESSOR	
3	EP 718758 A2	☒	Mechanism to identify instruction word boundaries in cache	
4	US 6175897 B	☒	Data processing system for pipelined computer central processor, sends instruction to pipeline from instruction buffer, if buffer target address matches with transfer instruction target address	
5	US 5734881 A	☒	Short Change-Of-Flow detection scheme processor for detecting COF instruction and target instruction are in pre-fetch buffer - has Branch Target Cache which outputs target data in accessed COF entry to pre-fetch unit, and pre-fetch unit which suppresses issue of corresp pre-fetch address if pre-fetch buffer field is valid	
6	EP 927394 B	☒	Branch prediction for a microprocessor instruction cache - has a branch target buffer which shares locations among sets of an instruction cache to store branch information for multiple branch instructions, when a cache line of a set stores more than one branch instruction	
7	US 5553254 A	☒	First-in-first-out queue for managing instruction sequence execution - has fields provided in queue element structure for referencing correct instruction cache line but also for specifying cache line sub-sequences and location of branch instructions	
8	EP 718758 A	☒	Cache control unit - includes boundary identification logic to determine nature of byte and anticipation buffer loaded with sequentially anticipated prefetched instructions	
9	JP 08077000 A	☒	Computer memory system super scalar microprocessor - has pre-prohibition circuit that controls execution circuit so that pre-buffer corresp. to pre-prohibition signal from cache command is forbidden	
10	RD 342024 A	☒	Instruction cache accessing method during reload sequence - using cache reload buffer equal to line size of instruction cache to access instruction cache during reload allowing processor to immediately access cache	
11	US 5230068 A	☐	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	

	Document ID	U	Title	Current OR
1	US 20030 23362 5 A1	☐	Method for allocating spare cells in auto-place-route blocks	716/8
2	US 20030 08427 3 A1	☒	Processor and method of testing a processor for hardware faults utilizing a pipeline interlocking test instruction	712/227
3	US 20030 03350 5 A1	☒	Apparatus for processing instructions in a computing system	712/215
4	US 20030 00526 2 A1	☒	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
5	US 20020 19446 4 A1	☒	Speculative branch target address cache with selective override by seconday predictor based on branch instruction type	712/239
6	US 20020 19446 3 A1	☒	Speculative hybrid branch direction predictor	712/239
7	US 20020 19446 2 A1	☒	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
8	US 20020 19446 1 A1	☒	Speculative branch target address cache	712/238
9	US 20020 19446 0 A1	☒	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
10	US 20020 18883 4 A1	☒	Apparatus and method for target address replacement in speculative branch target address cache	712/238
11	US 20020 18883 3 A1	☒	Dual call/return stack branch prediction system	712/236
12	US 20020 09992 6 A1	☒	Method and system for prefetching instructions in a superscalar processor	712/207
13	US 20020 09191 6 A1	☒	Embedded-DRAM-DSP architecture	712/228
14	US 20020 08784 9 A1	☒	Full multiprocessor speculation mechanism in a symmetric multiprocessor (smp) System	712/235
15	US 20020 08784 5 A1	☒	Embedded-DRAM-DSP architecture	712/228
16	US 20020 04042 9 A1	☒	Embedded-DRAM-DSP architecture	712/228
17	US 20010 05413 7 A1	☒	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11

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18	US 20010037444 A1	☒	INSTRUCTION BUFFERING MECHANISM	712/207
19	US 6691221 B2	☒	Loading previously dispatched slots in multiple instruction dispatch buffer before dispatching remaining slots for parallel execution	712/215
20	US 6678820 B1	☒	Processor and method for separately predicting conditional branches dependent on lock acquisition	712/239
21	US 6658558 B1	☒	Branch prediction circuit selector with instruction context related condition type determining	712/239
22	US 6658534 B1	☒	Mechanism to reduce instruction cache miss penalties and methods therefor	711/137
23	US 6647467 B1	☒	Method and apparatus for high performance branching in pipelined microsystems	711/140
24	US 6604191 B1	☒	Method and apparatus for accelerating instruction fetching for a processor	712/207
25	US 6553482 B1	☒	Universal dependency vector/queue entry	712/216
26	US 6553480 B1	☒	System and method for managing the execution of instruction groups having multiple executable instructions	712/23
27	US 6535973 B1	☒	Method and system for speculatively issuing instructions	712/218
28	US 6523050 B1	☒	Integer to floating point conversion using one's complement with subsequent correction to eliminate two's complement in critical path	708/204
29	US 6499123 B1	☒	Method and apparatus for debugging an integrated circuit	714/724
30	US 6490606 B1	☒	Rounding denormalized numbers in a pipelined floating point unit without pipeline stalls	708/497
31	US 6477640 B1	☒	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
32	US 6442681 B1	☒	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
33	US 6415308 B1	☒	Converting negative floating point numbers to integer notation without two's complement hardware	708/204
34	US 6405232 B1	☒	Leading bit prediction with in-parallel correction	708/505
35	US 6393546 B1	☒	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
36	US 6381622 B1	☒	System and method of expediting bit scan instructions	708/211
37	US 6349381 B1	☒	Pipelined instruction dispatch unit in a superscalar processor	712/215
38	US 6332191 B1	☒	System for canceling speculatively fetched instructions following a branch mis-prediction in a microprocessor	712/240
39	US 6308259 B1	☒	Instruction queue evaluating dependency vector in portions during different clock phases	712/214

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40	US 62667 63 B1	☒	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
41	US 62667 52 B1	☒	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
42	US 62533 16 B1	☒	Three state branch history using one bit in a branch prediction mechanism	712/239
43	US 62471 24 B1	☒	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
44	US 62471 06 B1	☒	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	711/203
45	US 62370 85 B1	☒	Processor and method for generating less than (LT), Greater than (GT), and equal to (EQ) condition code bits concurrent with a logical or complex operation	712/223
46	US 62328 72 B1	☒	Comparator	340/146 .2
47	US 62302 62 B1	☒	Processor configured to selectively free physical registers upon retirement of instructions	712/244
48	US 62197 73 B1	☒	System and method of retiring misaligned write operands from a write buffer	711/201
49	US 62126 29 B1	☒	Method and apparatus for executing string instructions	712/241
50	US 62126 23 B1	☒	Universal dependency vector/queue entry	712/216
51	US 62126 22 B1	☒	Mechanism for load block on store address generation	712/216
52	US 62055 60 B1	☒	Debug system allowing programmable selection of alternate debug mechanisms such as debug handler, SMI, or JTAG	714/34
53	US 61924 65 B1	☒	Using multiple decoders and a reorder queue to decode instructions out of order	712/212
54	US 61758 97 B1	☒	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
55	US 61579 98 A	☒	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
56	US 61579 88 A	☒	Method and apparatus for high performance branching in pipelined microsystems	711/140
57	US 61417 47 A	☒	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
58	US 61382 30 A	☒	Processor with multiple execution pipelines using pipe stage state information to control independent movement of instructions between pipe stages of an execution pipeline	712/216
59	US 61227 27 A	☒	Symmetrical instructions queue for high clock frequency scheduling	712/214
60	US 61226 56 A	☒	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	718/100
61	US 61192 23 A	☒	Map unit having rapid misprediction recovery	712/244
62	US 61192 20 A	☒	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235

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63	US 6108775 A	☒	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
64	US 6079005 A	☒	Microprocessor including virtual address branch prediction and current page register to provide page portion of virtual and physical fetch address	711/213
65	US 6079003 A	☒	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
66	US 6076146 A	☒	Cache holding register for delayed update of a cache line into an instruction cache	711/125
67	US 6073231 A	☒	Pipelined processor with microcontrol of register translation hardware	712/218
68	US 6035390 A	☒	Method and apparatus for generating and logically combining less than (LT), greater than (GT), and equal to (EQ) condition code bits concurrently with the execution of an arithmetic or logical operation	712/220
69	US 6035387 A	☒	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
70	US 6016545 A	☒	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
71	US 5960071 A	☒	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
72	US 5833021 A	☒	Cache holding register for receiving instruction packets and for providing the instruction packets to a predecode unit and instruction cache	711/125
73	US 5742760 A	☒	Data processor to control a sequence of instructions to be executed by rearranging the instruction blocks	712/32
74	US 5639084 A	☒	Address translation unit employing programmable page size	711/206
75	US 5580042 A	☒	Grouping logic circuit in a pipelined superscalar processor	712/215
76	US 5548715 A	☒	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
77	US 5481000 A	☒	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
78	US 5467005 A	☒	Avoidance of cache synonyms	711/108
79	US 5444817 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/240
80	US 5371778 A	☒	Register file for registers with multiple addressable sizes using read-modify-write for register file update	712/218
81	US 5352241 A	☒	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
82	US 5918005 A	☒	Apparatus region-based detection of interference among reordered memory operations in a processor	714/38
83	US 5907860 A	☒	System and method of retiring store data from a write buffer	711/117
84	US 5903751 A	☒	Method and apparatus for implementing a branch target buffer in CISC processor	712/238

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85	US 5857089 A	☒	Floating point stack and exchange instruction	712/222
86	US 5842008 A	☒	Method and apparatus for implementing a branch target buffer cache with multiple BTB banks	712/240
87	US 5838897 A	☒	Debugging a processor using data output during idle bus cycles	714/30
88	US 5835967 A	☒	Adjusting prefetch size based on source of prefetch address	711/213
89	US 5835951 A	☒	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
90	US 5835949 A	☒	Method of identifying and self-modifying code	711/135
91	US 5805879 A	☒	In a pipelined processor, setting a segment access indicator during execution stage using exception handling	712/244
92	US 5794026 A	☒	Microprocessor having expedited execution of condition dependent instructions	712/236
93	US 5784589 A	☒	Distributed free register tracking for register renaming using an availability tracking register associated with each stage of an execution pipeline	712/217
94	US 5784586 A	☒	Addressing method for executing load instructions out of order with respect to store instructions	712/216
95	US 5781753 A	☒	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
96	US 5774710 A	☒	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
97	US 5771365 A	☒	Condensed microaddress generation in a complex instruction set computer	712/205
98	US 5768575 A	☒	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
99	US 5764938 A	☒	Resynchronization of a superscalar processor	712/200
100	US 5752274 A	☒	Address translation unit employing a victim TLB	711/206
101	US 5748976 A	☒	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
102	US 5748932 A	☒	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
103	US 5742755 A	☒	Error-handling circuit and method for memory address alignment double fault	714/53
104	US 5740416 A	☒	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
105	US 5740415 A	☒	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238

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106	US 5740398 A	☒	Program order sequencing of data in a microprocessor with write buffer	711/117
107	US 5734881 A	☒	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
108	US 5732253 A	☒	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
109	US 5732243 A	☒	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
110	US 5708788 A	☒	Method for adjusting fetch program counter in response to the number of instructions fetched and issued	712/214
111	US 5706492 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/238
112	US 5706491 A	☒	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
113	US 5701448 A	☒	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
114	US 5696955 A	☒	Floating point stack and exchange instruction	712/222
115	US 5692168 A	☒	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
116	US 5687110 A	☒	Array having an update circuit for updating a storage location with a value stored in another storage location	365/154
117	US 5649225 A	☒	Resynchronization of a superscalar processor	712/23
118	US 5644741 A	☒	Processor with single clock decode architecture employing single microROM	712/200
119	US 5630149 A	☒	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
120	US 5623615 A	☒	Circuit and method for reducing prefetch cycles on microprocessors	712/238
121	US 5623614 A	☒	Branch prediction cache with multiple entries for returns having multiple callers	712/240
122	US 5615402 A	☒	Unified write buffer having information identifying whether the address belongs to a first write operand or a second write operand having an extra wide latch	712/38
123	US 5611071 A	☒	Split replacement cycles for sectored cache lines in a 64-bit microprocessor interfaced to a 32-bit bus architecture	711/133
124	US 5604909 A	☒	Apparatus for processing instructions in a computing system	712/208
125	US 5596740 A	☒	Interleaved memory conflict resolution with accesses of variable bank widths and partial return of non-conflicting banks	711/157
126	US 5596735 A	☒	Circuit and method for addressing segment descriptor tables	712/239
127	US 5596731 A	☒	Single clock bus transfers during burst and non-burst cycles	710/305
128	US 5584009 A	☒	System and method of retiring store data from a write buffer	711/117

	Document ID	U	Title	Current OR
129	US 5574871 A	☒	Method and apparatus for implementing a set-associative branch target buffer	712/200
130	US 5553255 A	☒	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
131	US 5471598 A	☒	Data dependency detection and handling in a microprocessor with write buffer	711/122
132	US 5454087 A	☒	Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT	712/240
133	US 5434985 A	☒	Simultaneous prediction of multiple branches for superscalar processing	712/240
134	US 5371864 A	☒	Apparatus for concurrent multiple instruction decode in variable length instruction set computer	712/206
135	US 5353426 A	☒	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
136	US 5283873 A	☒	Next line prediction apparatus for a pipelined computed system	712/207
137	US 5230068 A	☒	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137
138	US 5210831 A	☒	Methods and apparatus for insulating a branch prediction mechanism from data dependent branch table updates that result from variable test operand locations	712/240
139	US 4991080 A	☒	Pipeline processing apparatus for executing instructions in three streams, including branch stream pre-execution processor for pre-executing conditional branch instructions	712/206
140	US 4943908 A	☒	Multiple branch analyzer for prefetching cache lines	712/240
141	US 4926323 A	☐	Streamlined instruction processor	712/238